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MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
SAGAR, KRIPA	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 13

Application Number: 09/821,478
Filing Date: March 29, 2001
Appellant(s): NG, HUNG YIP

James E Howard
For Appellant

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EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/29/01

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is ambiguous.

Appellant states in the brief that the invention is directed to a method of forming a semiconductor device wherein an etching process is used to correct the bias ("offset") between nested and isolated features ("structures") presented by the *preceding lithographic process*; Appellant contrasts this with eliminating a bias between nested and isolated features generated in a *subsequent* *lithographic* step (Instant Brief: p.4; para 3).

The terms "etching" and "lithographic formation" and "structures" are clarified below and easily understood with reference to the attached figure.

As noted in the instant brief conventional **lithographic steps** comprise photoresist exposure and development. The photoresist may be positive or negative tone (wherein the exposed or unexposed areas of the photoresist are removed

respectively). The linewidth bias between nested and isolated patterns is opposite in character in the two resist types. The development may be carried by a wet process ("developing") or by dry plasma development, which also referred to as "etching". The patterning and development (etching) steps lead to a critical dimension (CD) bias or "offset" between closely spaced (also referred to as "dense" or "nested") features and isolated ("sparse" or "iso") features. This is the offset referred to by the Appellant in the instant brief (p.4; para. 2). This has been referred to as ***"print bias"*** by the Examiner and consistently used in the rejection below.

Following this, the layers underlying the photoresist are *etched* by plasma etching using the photoresist as an etching mask. Optionally, a hard mask may be etched in the underlayer and the photoresist may be removed at this stage. The etching process introduces a CD-bias. This may be (a) due to the bias already present in the photoresist mask used for etching (referred above and designated as *print bias* in the rejection below) and (b) differences in the rate of etching of nested and isolated features, for example, due to space charging effects in a plasma. This has been termed as "***etch bias***" in the rejection below.

The CD bias may be corrected by ***trimming* the photoresist mask**, prior to etching the underlayer. Here the "oversized" features (whether they are nested or isolated) are trimmed to the size of the desired CD using the differential etching rates of nested and isolated features (etch bias). The "structure" being corrected in this instance is primarily the photoresist. These are embodied in instant independent claims 1,8. This is shown in the lower left box of the attached figure.

Alternatively the etching of the underlayers may be carried out in a manner that compensates for the bias in the etching rates of nested and isolated features. Oversized features would be etched faster than features close to the CD. The "structure" in this instance would include the photoresist mask as well as the underlayers. These are embodied in claims 14,19 as shown on the right side of the attached figure.

In both instances, the etch rates of the nested and isolated features are designed to be different in the photoresist mask (if present), as well as in the underlayers.

In summary: The instant invention is directed to a process that corrects the CD bias *after resist* patterning. The etch rates of the nested and isolated patterns on the photoresist mask are made different to effect this correction (trimming) and is embodied in independent claim 1. Stated differently the *print bias* is corrected by trimming the *photoresist* (Instant specification Figs.2,3).

In a related process, a photoresist pattern is transferred to the polysilicon conductor (Fig.4, 5) without trimming. In this instance the *etch bias* of the conductor, is adjusted by the space charge effect. This is embodied in claim 14.

It will be shown below that the cited references teach both instances.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1,3,6-8,10-13 stand or fall together and that claims 4,5,14,16 and 18-20 stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6174818	Tao et al.	01-2001
5783101	Ma et al.	07-1998
6297166	Horak et al.	10-2001

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims: The original rejection, as presented, is reproduced below. The numbers in parentheses are column;line numbers in the patent under discussion.

1. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pat. 6174818 to Tao et al. in view of US Pat. 5783101 to Ma et al. and further in view of US Pat. 6297166 to Horak et al.

The invention discloses a method of compensating for nested-to-isolated pattern bias. Positive bias is compensated for by adding a sputtering component to the etch

chemistry, while negative bias is adjusted for by the electrical bias on the substrate ("space charge" effect).

The instant claims recite providing a structure with a first critical dimension (CD) and lithographically reducing the CD by an O2-containing trimming etch. The claims further recite correcting the CD-bias between nested and isolated features during a plasma-etch and the etching parameters for the process.

Tao teaches a method of narrowing gate electrodes on a device. The steps comprise (a) forming a stack layer and patterning the photoresist, (b) optionally trimming the resist pattern (c) etching the anti-reflection coating (ARC) and hardmask and trimming the hard mask to a sub-lithographic dimension (if not trimmed by the photoresist) and (d) etching the gate to the desired sub-lithographic dimension. These are shown in Figs. 2-6. Tao uses an O2-containing gas in the plasma etching process (3;43-52). Tao teaches a method of narrowing gate electrodes on a device. The steps comprise (a) forming a stack layer and patterning the photoresist, (b) optionally trimming the resist pattern (c) etching the anti-reflection coating and hardmask and trimming the hard mask to a sub-lithographic dimension (if not trimmed by the photoresist) and (d) etching the gate to the desired sub-lithographic dimension. These are shown in Figs. 2-6. Tao uses an O2-containing gas in the plasma etching process (3;43-52). Tao discloses that the use of NF3 as an etchant species is known in prior art(1;52-58)

It does not teach correcting for the CD-bias, the magnitude of the correction or the etching parameters used. It does not specify positive or negative resists. Tao's layers include an oxide layer and an ARC but do not contain TEOS.

Ma teaches that CD-bias or "profile microloading" is known in prior art (1;60-2;21). The prior-art process corrects for the microloading effect by adjusting the RF power (and hence the space charge). Note that the resist sputtering effect is also adjustable by adjusting the frequency of the RF power (2;32-64). Ma's invention discloses further adjusting the etch parameters to correct for the CD bias. These include lowering the frequency (Fig.5) and increasing the RF power (3;10-27). The system is operated at 0-100mT (5;45-49).

Ma does not specify positive or negative photoresists (claims 2,4) or the extent of lateral trimming (claim 5) by the etch.

The choice of the photoresist and the adjustment of the trim are uniquely determined by the process. These are based on empirical data and process control techniques instituted on the manufacturing line. This is also taught by Horak who provides the concept of trimming the resist and ARC (anti-reflective coating) to compensate for the nested-isolated *etching bias* of the gate (6;49-7;44). It teaches that nested-iso *print bias* is also corrected by this process (7;45-67). The etch chemistries are adjusted between the sputtering and etching species to bring about the variable etch rates (fig.5-8).

Horak, Ma and Tao solve the problem of etch bias and attempt to form narrow gates with consistent CDs. It would have been obvious to one of ordinary skill in the art

at the time the invention was made to compensate for the etch bias of nested and isolated lines by biasing the etch-masks, as taught by Horak, using the teachings of Ma and Horak to set the etching parameters in Tao's trimming process because Ma teaches that varying the above mentioned parameters reduces microloading and increases the process window (3;15-27) while Horak teaches that this facilitates the design process for producing consistent products (2;45-65).

(11) Response to Argument

Applicant has argued (B) that the references of Tao, Ma and Horak would not have been combined, by one of ordinary skill in the art at the time of the invention; and (C) that references do not teach each and every element of the rejected claims.

In support of the first line of argument, Appellant cites ACS hospital Systems Inc. v. Montefiore Hospital (instant brief: p.7) to show that there is no *"explicit teaching, suggestion or motivation to combine"* and then proceeds to argue that the references teach *"completely different subject matters"* (instant brief: p.8). It will be shown that Tao, Ma and Horak are analogous art and solve the same problem as the Appellant's using resist trimming (Tao and Horak) and space charge effect (Horak and Ma).

Appellant recognizes (Instant specification: p.1 – p.2;L.8) the criticality of controlling gate "length" (the *width* of the polysilicon conductive line below the gate oxide) of a transistor and notes that in achieving a higher density of transistors on a substrate with smaller dimensions , referred to as "scaling path" this is even more

critical (instant specification: p.4;11-14). The invention is directed to a process to reduce variations in the gate CD in nested and isolated areas.

Tao addresses the same problem of gate CD control (Tao: 1;9-14) and recognizes that as device density increases, the criticality of controlling the gate CD increases (Tao:1;15-20). It teaches that photoresist *trimming* to achieve gate CD control becomes difficult to implement (Tao:1;26-29). Prior art teaches that polymer deposition during etching (from organic materials such as photoresists and anti-reflective coatings {ARC}) contribute to the etch rate differences (Tao:1;44-51). Tao's solution comprises an inorganic ARC, which also serves as one layer of a hard mask (Tao:2;6-9) and trimming the photoresist with an O-plasma(Tao:2;14-17). The photoresist is removed after transferring the trimmed pattern to the hard mask layers. Thus Tao clearly addresses gate CD control in nested features. It does not *explicitly* address differential etching between nested and isolated features. However the CD of isolated features is controlled by the same etch as used for nested features and it would be illogical to control one feature dimension at the expense of another. One of ordinary skill in the art would recognize the inconsistency of the logic. This has also been *explicitly stated* by Horak. Horak states that it would be deleterious to the device to trim only isolated features without considering nested features (Horak: 6; 31-35). This is further explained stating "the nested to isolated etch bias cannot be adjusted without causing the nested etch bias to also decrease" (Horak: 6;43-46). More directly, Horak states "In addition, both nested and isolated lines will be etched at the same time – the isolated lines are etched faster than are nested lines, but both are etched" (Horak:2;17-

20). Appellant's argument that Tao does not teach reducing the bias between nested and isolated features is further untenable – because it is not possible to etch one without etching the other. Appellant's selective reading of Tao's teachings leads to false conclusions. Tao's figs.3-5 are similar to instant figs 2A-2B. It would be misleading to suggest that the *instant invention* is directed to the trimming of an isolated line based on instant Figs. 2A-2B.

Ma, admittedly, does not address gate CD control; but is directed to an analogous problem; namely, *linwewidth variations* in *conductor lines* in nested and isolated features when using photoresist masks. The etching process is the same as that of the instant invention using Oxygen reactive ion etching (O-RIE). That the phenomenon of space charge effect in etching a metal and polysilicon are same is evidenced by comparing Ma (Ma:2;8-21) and the instant specification (instant specification: p.13;9-18). Both describe the charge build up and lateral etching of the layers _above_ the conductor layer. Ma compensates for the space charge effect by adjusting the RF frequency of the RIE unit (Ma: abstract). A person of ordinary skill in the art would instantly recognize that etching _conductive underlayers_ such as polysilicon gates would pose the same problems as Ma's etching of nested and isolated _metal lines_. It may be noted that Ma and Tao are both related to device fabrication by the same lithographic processes. Appellant has selectively interpreted Ma's teachings to suggest divergent subject matter.

Horak deals with the same problems as Tao and Ma—etching nested and isolated lines on semiconductor devices (Horak:2;51-65). Horak teaches the basic

phenomenon of etching bias in Tao's plasma etching (Horak: 1;34-54) as well as Ma's RIE-etching (Horak:1;55-2;20). Horak uses Ma's O-RIE etching to trim the etch masks prior to etching the underlying polysilicon layer (Horak:3;11-15). However the space charge effect is mitigated by adjusting the "etching" and "sputtering " species in the gases (Horak: 3; 20-27). This is the same technique used in the instant invention. Note, further that Horak teaches the *equivalence* of metal conductor etching and polysilicon etching to control gate CD using O-RIE (Horak: 8; 44-50).

Thus Appellant's argument that they teach different matters is untenable and based on selective reading of individual references to draw misleading conclusions.

Appellant argues (instant brief: p.8) that Ma teaches "avoiding microloading" (Ma: 3;10-28) while Horak teaches "compensating for subsequent normal etching process to prevent a nested/isolated offset-effect" (Horak: 6;49-7;2). The two, it is argued, are incompatible because one circumvents the problem while another solves the problem. Again Appellant's selective reading of the references leads to erroneous conclusions.

Ma solves the problem of nested / iso offset in etching a *conductor layer* using a photoresist mask. It does so by adjusting the RF power and frequency such that the sputtering phenomenon and etching phenomenon are balanced ("space charge effect"). This leads to little or no re-deposition of the photoresist ("profile microloading") during the conductor etch. The reduction of microloading permits faster etching of nested features.

Horak similarly solves the problem of nested/iso offset in etching an underlayer using a photoresist mask (the resist mask is not shown in figures – Horak: 5;3-4). It uses the space charge effect in O-RIE similar to Ma and the instant invention. It adjusts the reactive components to balance the sputtering and etching phenomenon; this adjustment is similar to the instant invention. This etching step provides a mask layer with no *print bias* and thus *subsequent normal etching* of the conductor layer becomes feasible (Horak:6;49-7;2); it serves the same function as mask trimming. Horak clarifies the term "*normal etching*" to include differential etching of nested/iso features *under the mask* (Horak:6;21-36 & 9;6-33). This *critical distinction* was clarified earlier in section 5 and is elaborated in Horak (Horak: 7;24-67).

Thus the arguments that the references teach unrelated subject matters is shown to be based on selective reading of individual references. The clear and specific teachings of the references amply suggest the state of the art at the time the invention was made. They completely refute the suggestion of hindsight reasoning. In fact Appellant's claim to having *discovered a novel use* of the *space charge effect* to eliminate etch bias (instant specification: p.14; L.13-17) is proven wrong by Ma and Horak who teach diverse methods of utilizing the effect to correct an *etch bias*. The motivation for combining the teachings and the method of combining them to arrive at the present invention have been presented in the original rejection above. These include: same problem being solved by all references by similar methods; increased process window by Ma's process and better product design using Horak's teachings.

In the second line of argument (C), Appellant contends that the references do not teach each and every element of the instant claims and hence the combination, even if feasible, would not lead to the instant invention (Appeal Brief: p.8). It has been shown immediately above in this section that the references teach each and every element of the instant claims. Only a brief summary is provided below.

Appellant states " the present invention corrects for the nested/isolated offset from the previous lithographic formation, as opposed to correcting for any isolated nested offset which would otherwise result from a subsequent lithographic formation". The artful wording of this argument obscures the distinction between (i) the Appellant's process of trimming the resist pattern prior to etching the oxide and gate layer as shown in instant Figs.2, 3 and (ii) the process of etching the underlayers using the space charge effect as shown in instant Figs. 4,5 and described in the instant specification (instant specification:p.12-14). {see also attached figure for clarification}

Both Tao and Horak teach the elements of independent claims 1 and 8 wherein the correction for the nested/iso offset is made to the resist pattern by trimming. Tao uses O-plasma etching while Horak teaches O-RIE etching. In either instance the *print bias* between nested and iso features is reduced or eliminated *before* the underlayer is etched.

Ma and Horak teach the elements of claims, 14,19 wherein a photoresist pattern is used to etch a mask layer (Horak) and /or a conductive layer (Ma) --similar to Appellant's Fig.4, 5. The space charge effect is used to balance the sputtering and etching effects in dense and isolated areas. Horak teaches adjusting the gas

composition – as does the instant invention; while Ma teaches adjusting the power and RF frequency of the etching apparatus to arrive at the same balance. In both instances any CD bias present in the mask layer is corrected in etching the underlying layers, using a space charge effect.

Appellant argues that Ma does not teach reducing an offset in the photoresist. Referring to Fig.1 in Ma's teachings (which is prior art) Appellant notes that Ma does not even show any nested/iso offset!! Appellant then contends that Ma's invention is directed to a post-lithographic etch process and not related to the instant invention. (Instant Appeal Brief:p.10).

This argument is unconvincing. The language of claims 14,19 *conceals* the fact that the process makes no distinction between eliminating *print bias* and *etch bias*. The process steps as claimed comprise: forming a resist pattern with nested and isolated features; *etching the device with a space charge effect to compensate for the CD bias*.

In contrast the specification recites two etching stages wherein the resist, an ARC layer and an oxide layer are first etched to form a cavity.

"As shown, the TEOS, ARC, and photoresist are etched to form a cavity 450 therebetween (step 520)". (instant specification: p.12)

There is no reference to eliminating the CD bias (*print bias*) at this step. In other words the nested/offset bias is transferred to the oxide (TEOS) and ARC layers without correction of the lithographic effect. In the following stage the conductive polysilicon layer is etched *with a space charge effect* such that the nested areas etch faster than the isolated areas.

"During the polysilicon conductor (PC) hardmask 440 (e.g., having a

thickness on the order of about 500 .ANG. oxide) etch, ions 460 generated from the plasma (e.g., NF.sub.3/Ar) etch oxide into polysilicon film 410 with minimum selectivity. The mixture of the NF.sub.3 to the argon can be varied such that the charging effect depends upon the characteristics of the chemistry and such gases may exist in different pluralities. Other gases may be employed as well including an electron negative charge plasma capable of performing the polysilicon and oxide etch." (ibid)

and later it is stated:

"Due to both mask erosion and mask pull-back, nested features etch faster than isolated features, which compensate for the nested-isolated offset from negative photo resist process." (ibid)

and again

"Mask erosion occurs in that the etch in this aspect of the invention is not selective as in the first aspect of the invention. That is, this type of chemistry also etches the mask and both of the materials in a similar fashion. Thus, there is no selectivity as to any material in the etching." (ibid)

In other words the *space charge effect comes into play only in etching the polysilicon layer.* This is precisely the *etch bias* that Ma's invention teaches. Ma teaches adjusting the RF power and frequency to bring about this etch rate difference between nested and isolated features in the conductor layers. Horak teaches that such *etch bias* is "normal" in O-RIE etching and reduces the contribution of *print bias* by trimming the mask layer (including the ARC) before "normal" etching. Horak *adjusts the gas composition* to selectively etch the nested features faster.

The argument that the instant invention corrects nested/iso offset created by the "*preceding lithographic process*" whereas the references teach compensating for the nested /iso offset to be created in a "*subsequent lithographic process*" is deceptive and not borne out by the Appellant's specification. Stated differently, the Appellant would have us believe that the space charge effect would correct *solely for the print*

bias but would not correct for the etch bias between nested and isolated features; *although the effect comes into play only during the etching of the gate conductor.*

Examples of similar logic can be seen in the argument that "none of the applied references even acknowledge correcting an existing offset" (Instant brief: p.11). Even one of ordinary skill in the art would readily recognize that Tao's and Horak's inventions teach correcting *print bias* in photoresist masks by trimming and Ma's invention teaches correcting *etch bias* by etching with a space charge effect.

In summary the instant references teach each and every element of the claims in contention and the motivation for combining the references has been explicitly stated in the rejection. Emphasis on "preceding lithographic process" and " subsequent lithographic process" obscures the fact that the embodiment of claims 1,8 namely *trimming a resist pattern*, is entirely obvious from Tao and Horak. The space charge effect of claims 14,19 comes into effect only in etching the conductor layer and is taught by Ma. The claimed "*novel use*" of this effect is neither novel nor unobvious as shown above.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Kripa Sagar
March 12 th 2004
Conferees

MARK F. HUFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

Mark Huff

Pat Ryan

MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817